the channel layer and composed of AlGaAs doped with n type impurities, an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP, a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities, a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP, a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer, a wide recess opening formed to penetrate the second contact layer so as to expose a surface of the recess stopper layer, a narrow recess opening formed in the wide recess opening to penetrate surfaces of the recess stopper layer, the first contact layer, and the electric field strength reducing layer so as to expose the surface of the first electron supply layer, a gate electrode provided on the surface of the first electron supply layer exposed from a bottom of the narrow recess opening, and a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

[0012] According to another aspect of the present invention, a manufacturing method for a heterojunction type compound semiconductor field effect transistor comprises forming a channel layer composed of intrinsic GaAs or InGaAs on a compound semiconductor substrate, forming a first electron supply layer composed of AlGaAs on the channel layer, forming an electric field strength reducing layer composed of intrinsic InGaP on the electron supply layer, forming a first contact layer composed of GaAs or InGaAs doped with n type impurities, on the electric field strength reducing layer, forming a recess stopper layer composed of intrinsic InGaP, on the first contact layer, forming, on the recess stopper layer, a second contact layer composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer, wet-etching the second contact layer to form a wide recess opening penetrating the second contact layer using the recess stopper layer as a stopper, forming a source electrode and a drain electrode on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode, wet-etching the first contact layer in the wide recess opening using the electric field strength reducing layer as a stopper, wet-etching the electric field strength reducing layer in the wide recess opening to form a narrow recess opening penetrating the recess stopper layer, the first contact layer, and the electric field strength reducing layer using the first electron supply layer as a stopper, and forming a gate electrode on a surface of the first electron supply layer exposed from a bottom of the narrow recess opening.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0013] **FIG. 1** is a sectional view of the structure of a conventional heterojunction type compound semiconductor field effect transistor;

[0014] **FIG. 2** is a sectional view of the structure of a heterojunction type compound semiconductor field effect transistor according to a first embodiment of the present invention;

[0015] **FIG. 3** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a first manufacturing step;

[0016] **FIG. 4** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a second manufacturing step;

[0017] **FIG. 5** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a third manufacturing step;

[0018] **FIG. 6** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a fourth manufacturing step;

[0019] **FIG. 7** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a fifth manufacturing step;

[0020] **FIG. 8** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a sixth manufacturing step;

[0021] **FIG. 9** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a seventh manufacturing step;

[0022] **FIG. 10** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing an eighth manufacturing step;

[0023] **FIG. 11** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a ninth manufacturing step;

[0024] **FIG. 12** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a tenth manufacturing step;

[0025] **FIG. 13** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing an eleventh manufacturing step;

[0026] **FIG. 14** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a twelfth manufacturing step;

[0027] **FIG. 15** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a thirteenth manufacturing step;

[0028] **FIG. 16** is a sectional view of the structure of the heterojunction type compound semiconductor field effect transistor according to the first embodiment of the present invention, showing a fourteenth manufacturing step;

[0029] **FIG. 17** is a sectional view of the structure of a heterojunction type compound semiconductor field effect transistor according to a second embodiment of the present invention;